CLAIMS

A wireless receiver, comprising:

at least one antenna for receiving a plurality of frames in a form of a plurality of paths;

wherein each of the plurality of frames comprises a plurality of time slots;

wherein each of the plurality of time slots comprises a plurality of symbols;

wherein each of the plurality of paths has a corresponding sample position; and

wherein the plurality of symbols comprise a primary synchronization code symbol;

circuitry for correlating a primary synchronization code across a group of the plurality of symbols;

circuitry for identifying a plurality of path positions within the group, wherein each of the plurality of path positions corresponds to a respective one of a plurality of largest-amplitude paths represented within the group as detected in response to the circuitry for correlating;

circuitry for defining a plurality of sub-windows;

wherein each of the plurality of sub-windows comprises a plurality of sample positions; and

wherein each of the plurality of sub-windows includes at least one of the plurality of identified path positions; and

circuitry for combining paths selected from the sample positions within the plurality of sub-windows.

2. The wireless receiver of claim 1 wherein the circuitry for combining comprises circuitry for despreading the selected paths.

3. The wireless receiver of claim 2 wherein the circuitry for combining comprises:

circuitry for estimating a channel estimate for each of the selected paths; and

rake receiver circuitry for combining the selected paths in response to the channel estimate for each of the selected paths.

4. The wireless receiver of claim 2 wherein the circuitry for combining comprises a joint detector for combining the selected paths.

5. The wireless receiver of claim 1:

wherein the group of the plurality of symbols has a duration equal to a duration of each of the plurality of time slots; and

wherein the plurality of path positions are within a time window having a duration less than the duration of each of the plurality of time slots.

6. The wireless receiver of claim 5 wherein the plurality of path positions are within a time window having a duration equal to one-tenth the duration of each of the plurality of time slots.

7. The wireless receiver of claim 5:

wherein the plurality of sub-windows consists of eight sub-windows; and

wherein each of the plurality of sub-windows consists of four sample positions.

8. The wireless receiver of claim 7 and further comprising circuitry for performing a delay profile estimation across each of the plurality of sample positions of each of the plurality of sub-windows, wherein the selected paths are selected in response to the delay profile estimation.

9. The wireless receiver of claim 5 and further comprising circuitry for performing a delay profile estimation across each of the plurality of sample positions of each of the plurality of sub-windows, wherein the selected paths are selected in response to the delay profile estimation.

10. The wireless receiver of claim 9 wherein the circuitry for performing a delay profile estimation correlates pilot symbols to each of the plurality of sample positions of each of the plurality of sub-windows.

11. The wireless receiver of claim 9 wherein the circuitry for performing a delay profile estimation correlates pilot and data/control symbols to each of the plurality of sample positions of each of the plurality of sub-windows.

12. The wireless receiver of claim 9:

wherein the circuitry for performing a delay profile estimation coherently correlates pilot symbols to each of the plurality of sample positions of each of the plurality of sub-windows; and

wherein the circuitry for performing a delay profile estimation noncoherently correlates data/control symbols to each of the plurality of sample positions of each of the plurality of sub-windows.

13. The wireless receiver of claim 5:

wherein the plurality of sub-windows is a first number of sub-windows;

wherein the plurality of sample positions is a second number of sample positions; and

wherein a product of the first number times the second number is less than a number of sample positions in the time window.

14. The wireless receiver of claim 13 wherein the circuitry for combining comprises circuitry for despreading the selected paths.

15. The wireless receiver of claim 14 wherein the circuitry for combining selected paths comprises:

circuitry for estimating a channel estimate for each of the selected paths; and

rake receiver circuitry for combining the selected paths in response to the channel estimate for each of the selected paths.

16. The wireless receiver of claim 14 wherein the circuitry for combining comprises a joint detector for combining the selected paths.

17. The wireless receiver of claim 1 and further comprising circuitry for performing a delay profile estimation across each of the plurality of sample positions of each of the plurality of sub-windows, wherein the selected paths are selected in response to the delay profile estimation.

18. The wireless receiver of claim 17 wherein the circuitry for performing a delay profile estimation correlates pilot symbols to each of the plurality of sample positions of each of the plurality of sub-windows.

19. The wireless receiver of claim 1:

wherein the plurality of sub-windows is a first number of sub-windows;

wherein the plurality of sample positions is a second number of sample positions; and

wherein a product of the first number times the second number is less than a number of sample positions in the time window.

20. The wireless receiver of claim 1 wherein the plurality of frames comprise time division duplex frames.

21. The wireless receiver of claim 1 wherein the plurality of frames comprise frequency division duplex frames.

22. The wireless receiver of claim 1 wherein the receiver comprises a CMDA receiver.

23. The wireless receiver of claim 1 wherein the receiver comprises a WCMDA receiver.

24. A method of operating a wireless receiver, comprising the steps of:

receiving a plurality of frames in a form of a plurality of paths along at least one antenna;

wherein each of the plurality of frames comprises a plurality of time slots;

wherein each of the plurality of time slots comprises a plurality of symbols;

wherein each of the plurality of paths has a corresponding sample position; and

wherein the plurality of symbols comprise a primary synchronization code symbol;

correlating a primary synchronization code across a group of the plurality of symbols;

identifying a plurality of path positions within the group, wherein each of the plurality of path positions corresponds to a respective one of a plurality of largest-amplitude paths represented within the group as detected in response to the circuitry for correlating;

defining a plurality of sub-windows;

wherein each of the plurality of sub-windows comprises a plurality of sample positions; and

wherein each of the plurality of sub-windows includes at least one of the plurality of identified path positions; and

combining paths selected from the sample positions within the plurality of sub-windows.

25. The method of claim 24 wherein the combining step comprises despreading the selected paths.

26. The method of claim 24 and further comprising the step of performing a delay profile estimation across each of the plurality of sample positions of each of the plurality of sub-windows, wherein the selected paths are selected in response to the delay profile estimation.

27. The method of claim 26 wherein the delay profile estimation correlates pilot symbols to each of the plurality of sample positions of each of the plurality of sub-windows.

28. The method of claim 24:

wherein the plurality of sub-windows is a first number of sub-windows;

wherein the plurality of sample positions is a second number of sample positions; and

wherein a product of the first number times the second number is less than a number of sample positions in the time window.

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